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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,389	12/31/2003	Tony Albrecht	5367-65	8976

7590 10/20/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,389	ALBRECHT ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 Sept. 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 22 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5822347 to Yokogawa et al.

Regarding claim 1, Yokogawa discloses a light-emitting diode chip in fig. 1 having an epitaxial semiconductor layer sequence 1012, col. 8 line 6, with an active zone 1015, column 8 line 10, that emits electromagnetic radiation and an electrical contact structure comprising a radiation-transmissive electrical current expansion layer 1019, which contains ZnO, column 8 line 24, and an electrical connection layer 1110/1018, column 8 line 17, wherein the current expansion layer 1019 is applied

directly on a cladding layer 1017, col. 8 line 15, of the semiconductor layer and comprises a window, in which the connection layer 1018 is applied directly on said cladding layer 1017 of the semiconductor layer sequence, the connection layer 1018 is electrically conductively connected to the current expansion layer 1019, and wherein junction between the connection layer 1018 and the cladding layer 1017, during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer 1018 flows via the current expansion layer 1019 into the semiconductor layer sequence.

Although the prior art does not specially disclose the during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor layer sequence limitation, this feature is seen to be inherently teaching of that limitation because Yokogawa discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 2, Yokogawa discloses the light-emitting diode chip according to claim 1, wherein the connection layer 1110/1018 comprises a metal, column 9 line 32, and the junction between the connection layer 1110/1018 and the cladding layer 1017 comprises an electrical potential barrier.

Regarding claims 3-4 and 22, Yokogawa discloses the light-emitting diode chip according to claim 1, the sheet resistance of intermediate layers of the semiconductor layer sequence between the active zone and the electrical contact structure is greater than or equal to 200 Ω /sq, wherein the current expansion layer 35 comprises a sheet resistance of less than or equal to 190 Ω /sq or 30 Ω/sp.

Although the prior art does not specially disclose the sheet resistance limitation, this feature is seen to be inherently teaching of that limitation because Yokogawa discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 5, Yokogawa discloses the light-emitting diode chip according to claim 1, wherein the connection layer 1110 extends beyond the window on a side of the current expansion layer 1019 which is remote from the semiconductor layer sequence and is applied to a front-side surface of the current expansion layer 35 so as to partly cover the current expansion layer 1019 and so that the junction between the connection layer 1110 and the current expansion layer 1019 is electrically conductive in this region, fig. 1.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6855570 to Takatani.

Regarding claim 1, Takatani discloses a light-emitting diode chip in fig. 5 having an epitaxial semiconductor layer sequence 104-108, col. 5 line 64, with an active zone 106, column 5 line 60, that emits electromagnetic radiation and an electrical contact structure comprising a radiation-transmissive electrical current expansion layer 110, which contains ZnO, col. 2 line 54 and col. 6 line 21, and an electrical connection layer 109//112, column 6 line 25, wherein the current expansion layer 110 is applied directly on a cladding layer 108, col. 5 line 63, of the semiconductor layer and comprises a window, in which the connection layer 109/112 is applied directly on said cladding layer 108 of the semiconductor layer sequence, the connection layer 109/112 is electrically conductively connected to the current expansion layer 110, and wherein junction between the connection layer 108/112 and the cladding layer 108, during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer 108 flows via the current expansion layer 110 into the semiconductor layer sequence 104-108.

Although the prior art does not specially disclose the during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor

layer sequence limitation, this feature is seen to be inherently teaching of that limitation because Yokogawa discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-5, 9-13, 22, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee et al. in view of US 6346719 to Udagawa et al.

Regarding claim 1, Lee discloses a light-emitting diode (LED) chip in fig. 3C having an epitaxial semiconductor layer sequence (31/32/33) with an active zone 32,

column 3 line 27, that emits electromagnetic radiation and an electrical contact structure (34/35/36) comprising a radiation-transmissive electrical current expansion layer 35 which contains ZnO, column 3 line 31, and an electrical connection layer 36, column 4 line 5, wherein the current expansion layer 35 is applied on a cladding layer of the semiconductor layer and comprises a window, in which the connection layer 36 is applied directly on said cladding layer 33, column 3 line 27, of the semiconductor layer sequence, the connection layer 36 is electrically conductively connected to the current expansion layer 35, and wherein junction between the connection layer 36 and the cladding layer 33, during the operation of the light-emitting diode chip, is not electrically conductive, column 3 line 3 line 60-65, or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer 36 flows via the current expansion layer 35 into the semiconductor layer sequence.

But, Lee does not disclose the current expansion layer is applied directly on a cladding layer.

However, Udagawa discloses a LED in fig. 5 comprises a cladding layer 305c, col. 7 line 20, a current expansion layer 306 containing ZnO, col. 7 line 25, is applied directly on the cladding layer 305c, fig. 5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the current expansion layer 306 teaching of Udagawa in with Lee's device, because it would have resulted in LED having an excellent monochromatic property as taught by Udagawa column 7 lines 50-55.

Although the prior art does not specially disclose the during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor layer sequence limitation, this feature is seen to be inherently teaching of that limitation because Lee discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent or obvious. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 2, Lee discloses the light-emitting diode chip according to claim 1, wherein the connection layer 36 comprises a metal, column 4 line 5, and the junction between the connection layer 36 and the cladding layer 33 comprises an electrical potential barrier, column 3 line 60-65.

Regarding claims 3-4, 22 Lee discloses the light-emitting diode chip according to claim 1, the sheet resistance of intermediate layers of the semiconductor layer sequence between the active zone and the electrical contact structure is greater than or equal to 200 Ω /sq, wherein the current expansion layer 35 comprises a sheet resistance of less than or equal to 190 Ω /sq or 30 Ω/sp.

Although the prior art does not specially disclose the sheet resistance limitation, this feature is seen to be inherently teaching of that limitation because Lee discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent or obvious. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 5, Lee discloses the light-emitting diode chip according to claim 1, wherein the connection layer 36 extends beyond the window on a side of the current expansion layer 35 which is remote from the semiconductor layer sequence (31/32/33) and is applied to a front-side surface of the current expansion layer 35 so as to partly cover the current expansion layer 35 and so that the junction between the connection layer 36 and the current expansion layer 35 is electrically conductive in this region, fig. 3C.

Regarding claims 9, 24 Lee discloses the light-emitting diode chip according to claim 1, wherein the layer p-type AlGaInP is doped with a dopant concentration of between about $1x10^{18}$, column 1 line 46.

Regarding to claims 10-13, 25-26 Lee discloses the current expansion layer 35 has general thickness.

But Lee does not discloses the current expansion layer comprises Al, wherein the proportion of Al between 0% and 10%, wherein the thickness between 100-600 nm or the thickness corresponding about a quarter of the wavelength of a radiation emitted by the light-emitting diode chip.

However, Udagawa discloses the light-emitting diode in fig. 6 wherein the expansion layer 406 comprises Al, column 8 line 56, wherein the proportion of Al between 0% and 10%, column 8 line 57, wherein the thickness between 100-600 nm, column 8 line 64. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ZnO:Al layer 406 teaching of

Udagawa with Lee's device, because Al doped ZnO would have created a specific resistance level for layer ZnO as taught by Udagawa, column 8 line 59.

9. Claim 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee et al. and US 6346719 to Udagawa et al. as applied to claim 1 above and further in view of US 6693352 to Huang et al.

Regarding claims 6, Lee discloses the light-emitting diode chip according to claim 1 wherein the semiconductor layer sequence is based on AlGaInP, column 25-28.

But Lee does not discloses the semiconductor layer $In_xGa_yAl_{1-x-y}P$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x + y \leq$

However, Huang discloses the semiconductor layer $Al_xGa_yIn_{1-x-y}P_{1-z}$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x + y \leq 1$, and $0 \leq z \leq 1$. Accordingly, it would have been obvious to one of ordinary skill in art to use the semiconductor layer teaching of Huang in Lee's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

10. Claims 7-8, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee et al. and US 6346719 to Udagawa et al. as applied to claim 1 above and further in view of US Pub 2003/0059972 to Ikeda et al.

Regarding claims 7, 23, Lee discloses the light-emitting diode chip according to claim 1, wherein the cladding layer 33 comprises AlGaInP, column 4 line 17.

But Lee does not disclose the cladding layer comprises $Al_xGa_{1-x}As_yP_{1-y}$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$ and where $0.1 \leq x \leq 0.5$ and $y = 1$ or where $x=0$ and $y=0$.

However, Ikeda discloses the cladding layer can comprise AlGaAs, GaInP, and AlGaInP [0033]. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to combine the cladding layer teaching of Ikeda to replace the cladding layer of Lee, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06. With respect to the x any y concentration, it would have been obvious to one of ordinary skill in art to combine the teaching of Lee and Ikeda in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 8, Lee does not discloses the light-emitting diode chip according to claim 7 wherein the cladding layer is p-doped with at least one of a the dopant Zn and C.

However, Lee discloses layer 33 is P-type cladding layer. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to understand that Zn would be a typical material used in the art as a dopant of p-type for cladding layer, see Wang (6469324) column 2 lines 26, Sasaki (6074889) column 1 lines 48-51, or Takeoka (5789773) column 1 line 61.

11. Claims 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee et al. and US 6346719 to Udagawa et al. as applied to claim 1 above and further in view of JP 2001036131 to Udagawa.

Regarding claims 14-21, Lee does not discloses the light emitting diode wherein the current expansion layer is provided with watertight material such that the current expansion layer is adequately protected against moisture, wherein watertight material is applied to free areas of the contact layer, wherein watertight material is applied to all the free areas of the contact layer, wherein the watertight material is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances Si_xN_y, SiO, SiO_2, Al_2O_3 and SiO_xN_y, 19, wherein a refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted so as to significantly minimized reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, wherein the current expansion layer has a thickness corresponding to about an integer multiple of half the wavelength of a radiation emitted by the light-emitting diode chip, and the watertight material has a thickness corresponding to about a quarter of said wavelength, wherein the thickness of the watertight material is in a range of between 50 and 200 nm inclusive.

However, Udagawa discloses the light emitting diode in fig. 1 wherein the current expansion layer 107 is provided with watertight material 108 in such a way that it is adequately protected against moisture, wherein watertight material is applied to free areas of the contact layer, wherein watertight material 108 is

applied to all the free areas of the contact layer, wherein the watertight material 108 is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances Si_xN_y, SiO, SiO_2, Al_2O_3 and SiO_xN_y, see abstract, wherein the refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted to the greatest possible extent in particular for a minimization of reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, see abstract, wherein the current expansion layer 107 has a general thickness, wherein the thickness of the watertight material 108 has a general thickness. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the watertight layer teaching of Udagawa with Lee's device, because it would have provided the protection and improved light emitting efficiency as taught by Udagawa, see abstract.

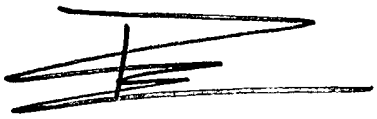
With respect to the thickness, it would have been obvious to one of ordinary skill in art to use the general thickness teaching of Udagawa with Lee's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
12 Oct. 2005